

# A 2-bit Miniature X-Band MEMS Phase Shifter

Guan-Leng Tan, Robert E. Mihailovich, Jonathan B. Hacker, *Member, IEEE*, Jeffrey F. DeNatale, *Member, IEEE*, and Gabriel M. Rebeiz, *Fellow, IEEE*

**Abstract**—The design and performance of a compact low-loss X-band true-time-delay (TTD) MEMS phase shifter fabricated on 8-mil GaAs substrate is described. A semi-lumped approach using microstrip transmission lines and metal-insulator-metal (MIM) capacitors is employed for the delay lines in order to both reduce circuit size as well as avoid the high insertion loss found in typical miniaturized designs [1], [2]. The 2-bit phase shifter achieved an average insertion loss of  $-0.70$  dB at 9.45 GHz, and an associated phase accuracy of  $\pm 1.3^\circ$ . It occupies an area of only  $5 \text{ mm}^2$ , which is 44% the area of the smallest known X-band MEMS phase shifter [3]. The phase shifter operates over 6–14 GHz with a return loss of better than  $-14$  dB.

**Index Terms**—Micromachining, radars, RF MEMS, switches, telecommunications.

## I. INTRODUCTION

MEMS phase shifters have received a lot of attention as an enabling technology for low-cost, high-performance passive phased arrays. The low-loss characteristic of MEMS phase shifters allows a single power amplifier to feed several antenna elements, each with its own phase shifter. This greatly reduces the cost, weight, and power dissipation of the phased array hardware, and is particularly attractive when a receive-only phased array is desired.

Conventional switched-line TTD phase shifters are limited in size due to the large space associated with the delay lines [4]. In multi-bit designs, much space is wasted due to the difficulty in optimizing the area occupied by delay lines of very different lengths [4]. This was partially solved by using SP4T switches [3], [5], but the size is still limited by the  $50 \Omega$  transmission-lines (t-lines).

Several attempts have been made in miniaturizing FET-based phase shifters by using embedded-FET or lumped approaches for the phase-delay networks [1], [2]. While such phase shifters achieve a very small size of  $1\text{--}2 \text{ mm}^2$ , the loss associated with the low- $Q$  on-chip inductors, as well as the transistor series resistance in the embedded-FET phase-shift networks, result in

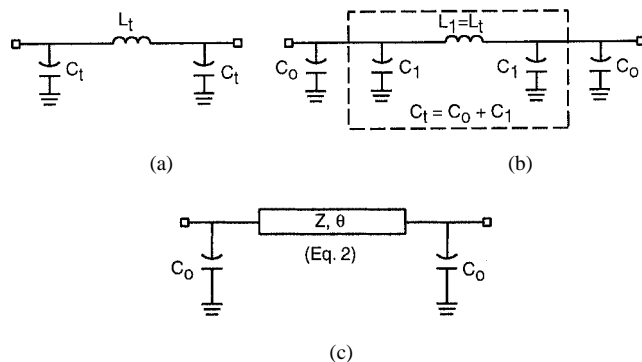


Fig. 1. (a) LC phase-shift network and (b) and (c) its transformation to a semi-lumped network.

phase shifters with relatively high losses ( $-5$  dB at 19 GHz for a 5-bit design [1]). Such approaches are therefore not suitable for use in the miniaturization of low-loss MEMS phase shifters.

In this work, a semi-lumped approach using t-lines and MIM capacitors is used to achieve a compact layout in the phase shifter. Tradeoff between size and loss is performed to obtain a design with minimal degradation in insertion loss compared to a traditional switched-line phase shifter. Also the phase shift network is designed to allow wideband operation using a cascade of smaller phase-shift sections.

## II. MODELING AND DESIGN

The phase shifter is realized on an 8-mil GaAs wafer with  $\epsilon_r = 12.9$ . The phase-shift network is derived from a series-L, shunt-C design and (1) presents the network phase shift ( $\phi$ ) in a matched condition [Fig. 1(a)]. As seen from (1), this network results in a maximum phase shift of  $-90^\circ$

$$\begin{aligned} X_n &\equiv \omega L / Z_o = -\sin \phi & (-90^\circ < \phi < 0) \\ B_n &\equiv \omega C Z_o = -\tan(\phi/2) & (-90^\circ < \phi < 0). \end{aligned} \quad (1)$$

Fig. 2 shows the return loss response of  $45^\circ$  and  $90^\circ$  lumped phase-delay networks designed at 10 GHz using (1), as well as that of two cascaded  $45^\circ$  delay networks. It is obvious that the cascaded response has a much broader bandwidth and a better phase linearity than a single  $90^\circ$  design, due to the increasing “distributed” nature of the circuit. A cascade of four  $22.5^\circ$  networks gives an even wider bandwidth, but the MIM capacitance becomes too small for implementation in the final design. The  $45^\circ$  section is therefore chosen as the basic building block for the design of the  $90^\circ$  and  $180^\circ$  delay networks.

In order to achieve a low-loss phase shifter, it is necessary to replace the lumped inductor in the  $45^\circ$  design with a low-loss t-line ( $Z, \theta$ ) and two MIM capacitors. This is done by breaking

Manuscript received August 6, 2002; revised October 8, 2002. This work was supported by AFRL under Contract F19628-00-C-0037, John Turtle Program Manager, and by Dr. John Smith and Dr. Larry Corey at DARPA Special Projects Office. The review of this letter was arranged by Associate Editor Dr. Shigeo Kawasaki.

G. L. Tan was with the Radiation Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122 USA. He is now with DSO National Laboratories, Singapore 118230 (e-mail: tguanlen@dso.org.sg).

R. E. Mihailovich, J. B. Hacker, and J. F. DeNatale are with Rockwell Scientific, Thousand Oaks, CA 91360 USA (e-mail: rmihailovich@rwsc.com; jhacker@rwsc.com; jdenatale@rwsc.com).

G. M. Rebeiz is with the Radiation Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122 USA (e-mail: rebeiz@umich.edu).

Digital Object Identifier 10.1109/LMWC.2003.811070

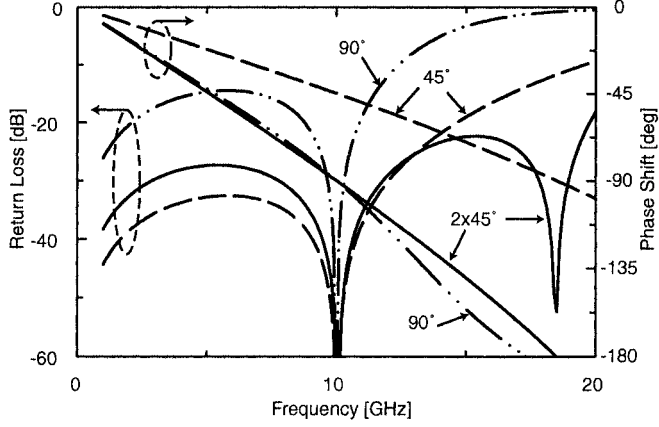


Fig. 2. (a) Return loss and (b) phase responses of 45°, 90°, and cascaded lumped-element phase shift networks.

the capacitance  $C_t$  into  $C_o$  and  $C_1$  [Fig. 1(b)], and the t-line  $Z$  and  $\theta$  are obtained by equating the  $S_{21}$  of the network comprising  $L_1$  and  $C_1$  [Fig. 1(b)] to the  $S_{21}$  of a lossless t-line [Fig. 1(c)]

$$1 - \omega^2 L_1 C_1 = \cos \theta$$

$$\sin \theta \cdot Z^2 - \omega Z [Z_o^2 (2C_1 - \omega^2 C_1^2 L_1) + L_1] + Z_o^2 \sin \theta = 0. \quad (2)$$

The value of  $C_o$  can be arbitrarily chosen ( $C_t < C_o < 0$ ), but a high value of  $C_o$  results in a narrow, high impedance t-line for the same phase shift, causing a high conductor loss. Therefore a moderate-width t-line ( $Z = 55\text{--}65 \Omega$ ) is chosen to minimize the insertion loss, while keeping the MIM capacitor values ( $C_o$ ) large enough for MMIC fabrication.

The 90° and the 180° phase delay networks in the 2-bit phase-shifter are configured using two and four sections of the 45° design, respectively (Fig. 3). After taking into account the effect of the bends and the via holes (see below), the 45° building blocks of the 90° and the 180° networks are  $Z = 63 \Omega$ ,  $C_o = 48$  fF, and  $Z = 58 \Omega$ ,  $C_o = 60$  fF, respectively.

Each delay network is connected to two SP2T switches, designed using three Rockwell Scientific MEMS series switches [5]. A typical back-to-back SP2T switch consists of four MEMS switches, but it is possible in this case to eliminate one of the two switches in the reference path since the t-line dimensions are electrically short at 10 GHz. As the input and output sections of the switch are narrow (40  $\mu\text{m}$ -wide), two open stubs are used to improve the impedance match in the reference state.

The 130  $\mu\text{m}$ -diameter RF via-hole used to connect the MIM capacitors to the microstrip ground are defined using deep RIE techniques, and has a simulated inductance of 62 pH (ADS Momentum). This results in an insignificant effect on the circuit since its impedance at 10 GHz is  $+j3.96 \Omega$ , which is much smaller than the impedance of the largest MIM capacitor (120 fF or  $-j132 \Omega$  at 10 GHz).

The MIM capacitors are implemented using 2000 Å-thick silicon nitride dielectric with an estimated  $\epsilon_r$  of 7.5. The capacitance is computed using the parallel-plate formula, plus 7–10% of fringing capacitance. The loss contribution due to the finite  $Q$  of the MIM capacitors is derived using lossy t-line formulas and is given by (3). The total MIM capacitance for the 90° delay

TABLE I  
SIMULATED LOSS BREAKDOWN OF THE 90° AND 180° SEMI-LUMPED PHASE DELAY NETWORKS (LAYOUT AS SHOWN IN FIG. 3) AT 10 GHz

Loss Component [dB]	90° network	180° network
Return Loss	−0.013	−0.002
Metal loss (Au, 2 $\mu\text{m}$ )	−0.308	−0.453
$R_s$ (1 $\Omega$ )	−0.189	−0.175
$Q$ (40)	−0.063	−0.160
Total Loss	−0.57	−0.79

network is 192 fF, which gives a loss of  $-0.063$  dB for a  $Q$  of 40. For the 180° design, the loss is  $-0.16$  dB since the total MIM capacitance is 480 fF

$$IL_{MIM} = 10 \log_{10} \frac{4[1 + 1/Q^2]}{[2/Q + \omega C Z_o]^2 + 4} \left( Q = \frac{1}{\omega C R_{s,MIM}} \right)$$

$$\simeq 10 \log_{10} \left[ 1 - \frac{\omega C Z_o}{Q} \right] (\omega C Z_o \ll Q). \quad (3)$$

Due to the complexity of the circuit, the phase shifter is designed using a combination of circuit and electromagnetic simulations. The 90° and 180° t-line networks (with the bends) are first simulated separately in ADS Momentum. The  $S$ -parameters obtained are then combined with lumped capacitors ( $Q = 40$  at 10 GHz) and the MIM values are adjusted to obtain the desired phase shift and good return loss. The SP2T switch networks and the interconnecting t-lines are also simulated using ADS Momentum to obtain the  $S$ -parameters in the various switch states. The MEMS bridge is ignored in the up-state simulation since its up-state capacitance is very small ( $< 2$  fF [5]). Finally, the  $S$ -parameters from the different simulations are combined in ADS to obtain the overall phase shifter performance in all 4-states, and the simulated loss breakdown of each bit is shown in Table I. The simulated average loss of the four states at 10 GHz is  $-0.90$  dB, and the return loss is  $-15$  dB or better from DC–16 GHz for both the input and output ports.

### III. FABRICATION AND MEASUREMENTS

The phase shifter is fabricated using the Rockwell Scientific MEMS process [5]. A photograph of the completed phase shifter is shown in Fig. 3. The circuit measures  $2.49 \text{ mm} \times 1.95 \text{ mm}$  ( $4.9 \text{ mm}^2$ ) and is only 44% the size of the smallest known MEMS 2-bit phase shifter [3].

A measured return loss of better than  $-14$  dB is obtained from 6–14 GHz (Fig. 4). The average measured insertion loss of the four states of the phase shifter is  $-0.70$  dB at 9.45 GHz, and  $-0.81$  dB over 6–14 GHz (Fig. 5). This compares favorably with the  $-0.6$  dB loss at 10 GHz for the low-loss SP4T phase shifter in [3]. The average on-state resistance of the MEMS switch, derived from the low frequency insertion loss measurement using  $IL = 20 \log_{10} [2Z_o / (2Z_o + R_s)]$ , is around  $1.2 \Omega$ . The difference between the measured and simulated losses is likely due to the piecemeal simulation approach, which ignores the coupling among the various circuit sections. Note that this phase shifter uses only six MEMS switches instead of eight in a typical 2-bit switched-line phase shifter, or the SP4T-based phase shifter [3].

Measurements indicate a wideband true-time delay response, centered around 9.45 GHz instead of the 10 GHz design

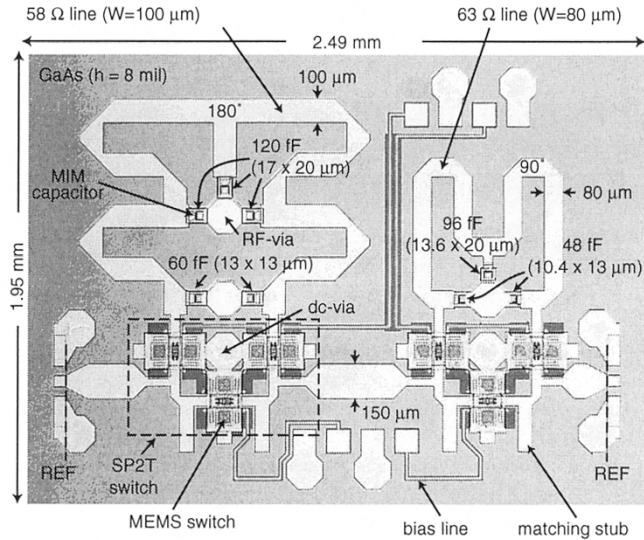


Fig. 3. Photograph of the completed 2-bit miniature MEMS phase shifter.

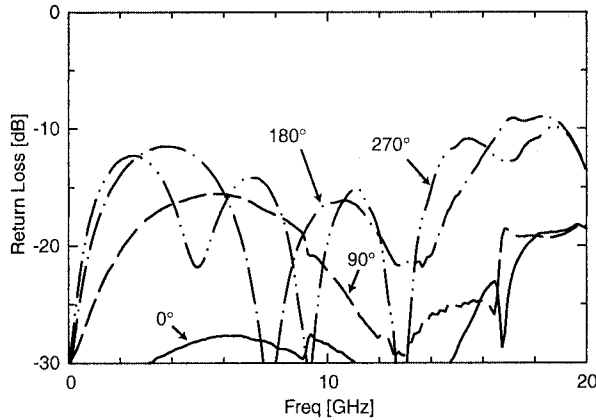


Fig. 4. Measured return loss of the 2-bit miniature MEMS phase shifter.

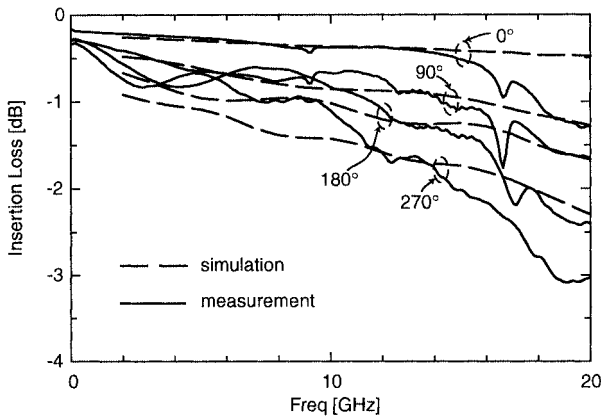


Fig. 5. Measured and simulated insertion loss of the 2-bit miniature MEMS phase shifter.

frequency. The differential phase shift at 9.45 GHz is  $88.7^\circ$ ,  $181.0^\circ$ , and  $269.4^\circ$  giving a phase accuracy of  $\pm 1.3^\circ$ . The frequency drift can be attributed to the lateral dimensional accuracy ( $\pm 1 \mu\text{m}$ ) of the physically small MIM capacitors,

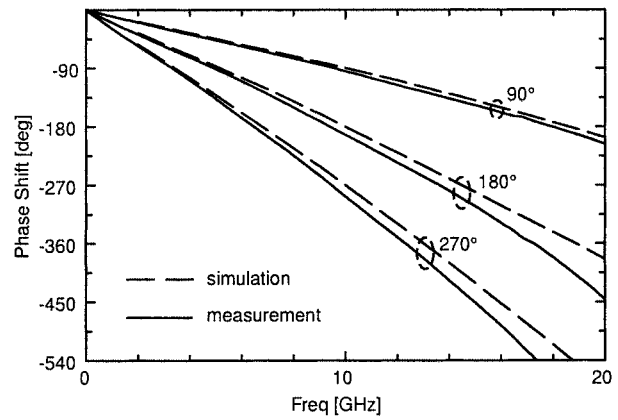


Fig. 6. Simulated and measured differential phase shifts of the 2-bit miniature MEMS phase shifter.

as well as the dielectric thickness accuracy ( $\pm 100\text{--}150 \text{ \AA}$  for  $2000\text{-\AA}$  thickness). Improvement in the accuracy of MIM capacitor values can be achieved by using metal-air-metal capacitors, which yield much larger capacitor dimensions and much less sensitivity to fabrication errors, in addition to a higher  $Q$  [6].

#### IV. CONCLUSION

The size of a 2-bit switched-line phase shifter has been successfully reduced using a semi-lumped approach for the delay lines. Phase bits designed using cascaded  $45^\circ$  phase-delay networks are shown to result in a wideband 6–14 GHz phase shifter, with excellent performance as compared to other low-loss MEMS phase shifters. The design center frequency of the phase shifter can be more precisely achieved with larger MIM capacitors or by using a metal-air-metal configuration.

#### ACKNOWLEDGMENT

The authors thank Dr. A. Brown, Picometrix Corp., for technical discussions and Dr. D. Pilz, Rockwell Scientific, for help on the X-band measurements.

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